POSTGRADUATE DEGREE COURSE

M. Tech. I to IV Semester

Electronics Engineering

(VLSI Design)

University of Technology

Vatika Road, Jaipur Rajasthan 303903

UNIVERSITY OF TECHNOLOGY, JAIPUR

Program Outcomes (POs)

PO 1	Engineering Knowledge: Apply knowledge of mathematics, science, and Civil, Computer Science, Electronics & Communication, Electrical, Mechanical engineering to solve numerical techniques problems.
PO 2	Problem Analysis: Identify, formulate, and solve Civil, Computer Science, Electronics & Communication, Electrical, Mechanical engineering problems.
PO 3	Design/Development of Solutions: Design and develop Civil, Computer Science, Electronics & Communication, Electrical, Mechanical engineering systems, components, or processes.
PO 4	Conduct Investigations: Conduct experiments and simulations to analyze Civil, Computer Science, Electronics & Communication, Electrical, Mechanical engineering problems.
PO 5	Modern Tool Usage: Use modern tools and software to analyze and solve Civil, Computer Science, Electronics & Communication, Electrical, Mechanical engineering problems.
PO 6	The Engineer and Society: Apply Civil, Computer Science, Electronics & Communication, Electrical, Mechanical engineering solutions to societal problems.
PO 7	Environment and Sustainability: Understand the impact of Civil, Computer Science, Electronics & Communication, Electrical, Mechanical engineering solutions on the environment.
PO 8	Ethics: Apply ethical principles to civil engineering practice.
PO 9	Individual and Team Work: Work effectively as an individual and in teams to solve civil engineering problems.
PO 10	Communication: Communicate Civil, Computer Science, Electronics & Communication, Electrical, Mechanical engineering ideas and solutions effectively.
PO 11	Project Management: Manage civil engineering projects and resources effectively.
PO 12	Lifelong Learning: Engage in lifelong learning to stay current with Civil, Computer Science, Electronics & Communication, Electrical, Mechanical engineering developments.

Program Specific Outcomes (PSOs)

1. **PSO 1**: Graduates will be able to design, simulate, and implement VLSI circuits, including digital and analog systems, using modern tools and techniques in the field of VLSI design.
2. **PSO 2**: Graduates will possess the ability to develop innovative solutions for complex problems in domain of VLSI with strong focus on optimization & performance enhancement.
3. **PSO 3**: Graduates will be proficient in using industry-standard VLSI design and verification software tools, understanding and applying advanced concepts in semiconductor technology, and demonstrating skills for real-world industrial applications.

Program Educational Objectives (PEOs)

1. **PEO 1**: To prepare graduates with a strong foundation in the theoretical and practical aspects of VLSI design, enabling them to contribute to the development of state-of-the-art electronic systems.
2. **PEO 2**: To equip graduates with the necessary skills to identify, analyze, and solve complex VLSI design challenges, ensuring they are capable of working in multidisciplinary teams and handling real-world industrial projects.
3. **PEO 3**: To nurture a spirit of innovation and research in VLSI design, encouraging graduates to pursue higher studies, contribute to cutting-edge research, and remain adaptable to the evolving technological landscape.
4. **PEO 4**: To provide graduates with professional ethics, communication skills, and an understanding of the impact of VLSI systems on society, empowering them to make informed decisions and become responsible leaders in the field of electronics engineering.

Course Overview and Objectives

The VLSI Design course aims to provide students with an in-depth understanding of the design, analysis, and digital VLSI systems. The course objectives are to equip students with the skills to design high-performance circuits and understand the manufacturing process involved in VLSI technology. The program also emphasizes the importance of semiconductor physics, CMOS technology, and the integration of these elements to build efficient and reliable VLSI systems. Students will develop expertise in using advanced techniques to address design challenges, ensuring they are prepared for careers in both research and industry within the rapidly evolving field of VLSI technology.

Scheme of

POSTGRADUATE DEGREE

COURSE

M. Tech

Electronics Engineering

(VLSI Design)

UNIVERSITY OF TECHNOLOGY, JAIPUR
Scheme and Syllabus

M.Tech 1st Year, I Sem: VLSI Design

Teaching and Examination Scheme
ACADEMIC SESSION 2023-2024

S. No.	Course Name	Contact Hours per Week			Marks				Cr
		L	T	P	Exam Hrs	IA	ETE	Total	
1	Advanced Mathematics	5	0	0	3	25	100	125	5
2	VLSI Design	5	0	0	3	25	100	125	5
3	Digital System Design	5	0	0	3	25	100	125	5
4	Micro-Electro-Mechanical-Systems	5	0	0	3	25	100	125	5
5	VLSI Physical Design Lab	0	0	4		60	40	100	2
	Total	**20**	**0**	**4**		**160**	**440**	**600**	**22**

L: *Lecture,* ***T:*** *Tutorial,* ***P:*** *Practical,* ***Cr:*** *Credits*
ETE: *End Term Exam,* ***IA:*** *Internal Assessment*
**: Not to be considered for award of division*

UNIVERSITY OF TECHNOLOGY, JAIPUR
Scheme and Syllabus
M.Tech 1st Year, II Sem: VLSI Design

Teaching and Examination Scheme
ACADEMIC SESSION 2023-2024

S. No.	Course Name	Contact Hours per Week			Marks				Cr
		L	T	P	Exam Hrs	IA	ETE	Total	
1	Digital Signal Processing	5	0	0	3	25	100	125	5
2	Analog & Mixed Signal ICs	5	0	0	3	25	100	125	5
3	CAD of ICs	5	0	0	3	25	100	125	5
4	Biomedical Electronics	5	0	0	3	25	100	125	5
5	Digital System Design Lab	0	0	4		60	40	100	2
	Total	**20**	**0**	**4**		**160**	**440**	**600**	**22**

***L:** Lecture, **T:** Tutorial, **P:** Practical, **Cr:** Credits*
***ETE:** End Term Exam, **IA:** Internal Assessment*
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UNIVERSITY OF TECHNOLOGY, JAIPUR
Scheme and Syllabus
M.Tech 2nd Year, III Sem: VLSI Design

Teaching and Examination Scheme
ACADEMIC SESSION 2023-2024

S. No.	Course Name	Contact Hours per Week			Marks				Cr
		L	T	P	Exam Hrs	IA	ETE	Total	
1	Embedded System Design	5	0	0	3	25	100	125	5
2	VLSI Testing & Testability	5	0	0	3	25	100	125	5
3	Seminar	0	0	0		90	60	150	6
4	Dissertation- I	0	0	0		100	0	100	4
	Total	**10**	**0**	**0**		**240**	**260**	**500**	**20**

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UNIVERSITY OF TECHNOLOGY, JAIPUR
Scheme and Syllabus
M.Tech 2nd Year, IV Sem: VLSI Design

Teaching and Examination Scheme
ACADEMIC SESSION 2023-2024

S. No	Course Name	Contact Hours per Week			Marks				Cr
		L	T	P	Exam Hrs	IA	ETE	Total	
1	Dissertation-II	0	0	0		500	0	500	16
	Total					**500**	**0**	**500**	**16**

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UNIVERSITY OF TECHNOLOGY, JAIPUR

Syllabus of

POSTGRADUATE DEGREE COURSE

M. Tech

Electronics Engineering

(VLSI Design)

UNIVERSITY OF TECHNOLOGY, JAIPUR
Scheme and Syllabus

M.Tech 1st Year, I Sem: VLSI Design

Teaching and Examination Scheme
ACADEMIC SESSION 2023-2024

S. No.	Course Name	Contact Hours per Week			Marks				Cr
		L	T	P	Exam Hrs	IA	ETE	Total	
1	Advanced Mathematics	5	0	0	3	25	100	125	5
2	VLSI Design	5	0	0	3	25	100	125	5
3	Digital System Design	5	0	0	3	25	100	125	5
4	Micro-Electro-Mechanical-Systems	5	0	0	3	25	100	125	5
5	VLSI Physical Design Lab	0	0	4		60	40	100	2
	Total	**20**	**0**	**4**		**160**	**440**	**600**	**22**

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UNIVERSITY OF TECHNOLOGY, JAIPUR

1st Year - I Semester: M. Tech. (VLSI Design)

Sub: Advanced Mathematics

Credit: 5 **Max. Marks**: 125 (IA:25, ETE:100)

5L+0T+0P **End Term Exam**: 3 Hours

S.No.	CONTENTS	CONTACT HOURS
1.	**Introduction**: Objective, scope, and outcome of the course.	01
2.	**Linear Algebra**: Vector spaces, basis and dimension, eigenvalues, eigenvectors, diagonalization, Gram-Schmidt orthogonalization, LU decomposition, QR decomposition, spectral theorem, matrix factorizations, and applications in signal processing and quantum computing.	07
3.	**Complex Analysis**: Analytic functions, conformal mapping, Cauchy's integral theorem, residue theorem, Laurent series, Taylor series, Riemann surfaces, poles and singularities, and applications in electromagnetic theory and fluid dynamics.	07
4.	**Numerical Methods**: Solutions of equations (bisection, Newton-Raphson), interpolation techniques (Lagrange, Hermite), numerical differentiation and integration (Gaussian quadrature), matrix inversion, eigenvalue computations, and optimization (gradient descent, least-squares fitting).	08
5.	**Probability and Statistics**: Probability axioms, joint distributions, conditional probability, Bayesian inference, hypothesis testing, confidence intervals, Markov processes, and stochastic simulations.	09
6.	**Advanced Calculus**: PDEs (wave, heat, Laplace), Green's and Stokes' theorems, calculus of variations (Euler-Lagrange equation), tensor calculus, and applications in structural mechanics and thermodynamics.	09
	Total	**41**

Text/Reference Books

1. **Erwin Kreyszig**, *Advanced Engineering Mathematics*, 10th Edition, Wiley India.
   - Comprehensive coverage of engineering mathematics topics with practical applications.
2. **B.S. Grewal**, *Higher Engineering Mathematics*, 44th Edition, Khanna Publishers.
   - Covers numerical methods, differential equations, and linear algebra extensively.
3. **Gilbert Strang**, *Linear Algebra and Its Applications*, 5th Edition, Wellesley-Cambridge Press.

- A foundational book for understanding linear algebra in applied contexts.

4. **R.K. Jain and S.R.K. Iyengar**, *Advanced Engineering Mathematics*, 6th Edition, Narosa Publishing House.
    - Detailed explanations of numerical techniques and engineering applications.
5. **Richard Bronson and Gabriel B. Costa**, *Schaum's Outline of Differential Equations*, 3rd Edition, McGraw Hill.
    - Problem-solving focus with numerous examples and exercises.

Course Outcomes (COs)

CO	Description
CO1	Apply linear algebra techniques in advanced engineering problems.
CO2	Utilize complex analysis in solving real-world physics and engineering challenges.
CO3	Implement numerical methods for approximating solutions to mathematical models.
CO4	Analyze and interpret data using probability and statistical methods.
CO5	Solve advanced calculus problems in the context of engineering applications.

Course Description

This course delves into advanced mathematical concepts such as linear algebra, complex analysis, numerical methods, probability, and statistics. These topics are framed in the context of real-world engineering applications, emphasizing analytical and computational skills to address complex challenges.

Course Objectives

1. Develop a strong foundation in applying advanced linear algebra and calculus for engineering applications.
2. Equip students with the knowledge to utilize numerical methods and complex analysis in problem-solving.
3. Enable the use of statistical and probability techniques to analyze and interpret engineering data.
4. Foster skills for applying mathematical concepts in designing and optimizing engineering systems.

CO-PO Mapping

Course Outcomes (CO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	1	2	1	-	-	-	-	-	-	3
CO2	3	2	-	1	2	-	-	-	2	-	-	2
CO3	3	3	-	2	3	-	1	-	2	-	-	1
CO4	3	2	2	3	2	-	-	-	-	2	-	1
CO5	3	3	3	2	2	-	-	-	-	-	-	3

CO-PSO Mapping

Course Outcomes (CO)	PSO1	PSO2	PSO3
CO1	3	2	-
CO2	2	2	-
CO3	3	-	-
CO4	-	-	2
CO5	3	2	2

UNIVERSITY OF TECHNOLOGY, JAIPUR

1st Year - I Semester: M. Tech. (VLSI Design)

Sub: VLSI Design

Credit: 5 **Max. Marks**: 125(IA:25, ETE:100)

5L+0T+0P **End Term Exam**: 3 Hours

S.No.	**CONTENTS**	**CONTACT HOURS**
1.	**Introduction**: Objective, scope, and outcome of the course.	01
2.	**Basic CMOS Technology**: Overview of MOSFET, threshold voltage, current-voltage characteristics, basic layout design, electrical and mechanical properties, scaling and Moore's Law, process variations, fabrication processes, CMOS process technology, and introduction to fabrication.	07
3.	**Combinational Logic Circuits**: CMOS logic gates (AND, OR, NOT, NAND, NOR), pass-transistor logic, transmission gates, logic optimization techniques, static CMOS logic design, power consumption analysis, propagation delay in CMOS circuits, logic synthesis, and low-power design techniques.	08
4.	**Sequential Circuits Design**: Flip-flops (SR, D, JK, T), latches, sequential circuit synthesis, registers, counters, timing analysis, clocking strategies, race conditions, hazards, setup and hold times, clock-skew analysis, state machine design and synthesis, and high-speed sequential circuit design.	08
5.	**Design of Arithmetic Circuits**: Adder circuits (Ripple carry adder, carry-lookahead adder, carry-save adder), multiplier circuits (array multiplier, Booth's multiplier, Wallace multiplier), division circuits, comparison circuits, ALU design, and optimized VLSI design of arithmetic functions.	08
6.	**VLSI Design for Performance and Power Optimization**: Power analysis and optimization, dynamic power consumption, leakage power, low-power design techniques, clock gating, voltage scaling, high-speed circuits, pipelining techniques, system-on-chip (SoC) design considerations, high-level synthesis, and design verification strategies.	08

Text/Reference Books

1. **Neil H.E. Weste and David Money Harris**, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th Edition, Pearson.
   - Detailed introduction to CMOS circuits and system-level VLSI design.
2. **Jan M. Rabaey**, *Digital Integrated Circuits: A Design Perspective*, 2nd Edition, Pearson.
   - Focuses on digital circuit design principles and practical insights.
3. **Douglas A. Pucknell and Kamran Eshraghian**, *Basic VLSI Design*, 3rd Edition, Prentice Hall.
   - Ideal for beginners to learn the fundamentals of VLSI.
4. **John P. Uyemura**, *Introduction to VLSI Circuits and Systems*, 1st Edition, Wiley.
   - A balance of theoretical and practical design aspects.
5. **Sung-Mo Kang and Yusuf Leblebici**, *CMOS Digital Integrated Circuits: Analysis and Design*, 4th Edition, McGraw Hill.

Course Outcomes (COs)

CO	Description
CO1	Design and optimize basic CMOS logic gates and combinational circuits for efficient performance.
CO2	Understand and apply various techniques in the design of sequential circuits, including flip-flops, latches, and state machines.
CO3	Develop and implement complex arithmetic units, such as adders and multipliers, with performance optimizations.
CO4	Utilize VLSI design techniques to optimize power consumption and enhance circuit performance.
CO5	Analyze and design complex integrated systems, including high-level design, verification, and power/performance trade-offs.

Course Description

This course introduces the fundamental principles and methodologies of Very Large Scale Integration (VLSI) design, focusing on CMOS technology. Topics include logic gate design, combinational and sequential circuit analysis, optimization techniques for power and performance, and system-level integration.

Course Objectives

1. Equip students with the ability to design and optimize CMOS-based circuits for various applications.
2. Provide knowledge of sequential circuit design and state machine analysis.

3. Develop proficiency in creating complex arithmetic and integrated systems with performance trade-offs.
4. Foster understanding of power-efficient VLSI design techniques and verification processes.

Mapping Table

The mapping table uses a scale of 1 to 3 to indicate the level of correlation between COs and POs/PSOs, where:

1. Slight (Low)
2. Moderate (Medium)
3. Substantial (High)

CO-PO Mapping

Course Outcomes (CO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	3	2	2	-	-	-	-	-	-	2
CO2	3	2	2	3	3	-	-	-	-	-	-	2
CO3	3	3	3	2	3	-	-	-	-	-	-	3
CO4	2	3	3	3	3	2	3	-	-	-	-	2
CO5	3	3	3	3	3	3	2	-	-	-	-	3

CO-PSO Mapping

Course Outcomes (CO)	PSO1	PSO2	PSO3
CO1	3	-	-
CO2	2	2	1
CO3	-	-	-
CO4	-	2	3
CO5	3	2	3

1st Year - I Semester: M. Tech. (VLSI Design)

Sub: Digital System Design

Credit: 5 **Max. Marks**: 125 (IA:25, ETE:100)

5L+0T+0P **End Term Exam**: 3 Hours

S.No.	CONTENTS	CONTACT HOURS
1.	**Introduction**: Objective, scope, and outcome of the course.	01
2.	**Boolean Algebra and Logic Minimization**: Logic synthesis techniques, Quine-McCluskey method, Karnaugh maps, heuristic methods, espresso algorithm, don't-care conditions, multi-level logic optimization, Reed-Muller expressions, and applications in digital systems.	07
3.	**Finite State Machines (FSMs)**: Classification of FSMs (Mealy and Moore), design of sequential circuits, timing analysis, race-free FSMs, metastability handling, reconfigurable FSMs, FSM minimization techniques, and synchronization issues in FSMs.	08
4.	**Digital Arithmetic**: High-speed adders (carry-lookahead, carry-save), multiplier architectures (Booth's algorithm, Wallace tree), division techniques, square root algorithms, IEEE-754 floating-point standard, arithmetic pipelines, and error detection in arithmetic units.	08
5.	**Hardware Description Languages (HDLs)**: Structural, behavioral, and dataflow modeling styles; Verilog/VHDL programming, testbench creation, simulation methodologies, synthesis constraints, debugging, FSM implementation, and mixed-signal modeling.	08
6.	**FPGA-Based System Design**: FPGA architecture overview, CLBs and interconnects, design flow for FPGAs, system-on-chip (SoC) design, AXI protocol, integration of soft IP cores, clock domain management, and real-time system implementation.	08

Text/Reference Books

1. **Charles H. Roth Jr. and Larry L. Kinney**, *Fundamentals of Logic Design*, 7th Edition, Cengage Learning.
   - A practical approach to logic design and its applications.
2. **Morris Mano and Michael D. Ciletti**, *Digital Design*, 5th Edition, Pearson.
   - A comprehensive guide to digital circuit design concepts and techniques.
3. **Stephen Brown and Zvonko Vranesic**, *Fundamentals of Digital Logic with VHDL Design*, 3rd Edition, McGraw Hill.
   - Integrates VHDL with digital logic design for modern systems.
4. **John F. Wakerly**, *Digital Design: Principles and Practices*, 4th Edition, Pearson.
   - Combines practical design principles with theoretical concepts.
5. **Samir Palnitkar**, *Verilog HDL: A Guide to Digital Design and Synthesis*, 2nd Edition, Pearson.
   - Focuses on Verilog HDL programming for digital systems.

Course Outcomes (COs)

CO	Description
CO1	Simplify and synthesize digital circuits using advanced Boolean algebra techniques.
CO2	Design robust and optimized FSMs for various digital system applications.
CO3	Implement high-speed digital arithmetic operations for computation-intensive applications.
CO4	Develop complex hardware systems using Verilog/VHDL for simulation and synthesis.
CO5	Design, simulate, and deploy FPGA-based digital systems for real-time applications.

Course Description

This course focuses on the principles and techniques for designing digital systems using advanced Boolean algebra, finite state machines (FSMs), and hardware description languages (HDLs). Emphasis is placed on optimizing performance, simulation, and deployment using FPGA technology.

Course Objectives

1. Provide in-depth understanding of Boolean algebra and its application in digital circuit simplification.
2. Enable students to design and optimize FSMs for various digital applications.
3. Equip learners with skills to implement high-speed digital arithmetic operations.
4. Foster proficiency in using Verilog/VHDL for simulation and synthesis.
5. Prepare students to design, simulate, and deploy FPGA-based systems for real-world applications.

Mapping Table

The mapping table uses a scale of 1 to 3 to indicate the level of correlation between COs and POs/PSOs, where:

1. Slight (Low)
2. Moderate (Medium)
3. Substantial (High)

CO-PO Mapping

Course Outcomes (CO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	2	2	-	-	-	-	-	-	3
CO2	3	3	3	3	3	-	-	-	2	-	-	3
CO3	3	3	3	2	3	-	-	-	-	-	-	3
CO4	3	3	3	3	3	-	-	-	2	2	-	3
CO5	3	3	3	3	3	2	2	-	2	2	3	3

CO-PSO Mapping

Course Outcomes (CO)	PSO1	PSO2	PSO3
CO1	3	2	2
CO2	3	3	2
CO3	3	3	3
CO4	3	3	3
CO5	3	3	3

UNIVERSITY OF TECHNOLOGY, JAIPUR

1st Year - I Semester: M. Tech. (VLSI Design)

Sub: Micro-Electro-Mechanical Systems (MEMS)

Credit: 5 **Max. Marks**: 125 (IA:25, ETE:100)

5L+0T+0P **End Term Exam**: 3 Hours

S.No.	CONTENTS	CONTACT HOURS
1.	**Introduction**: Objective, scope, and outcome of the course.	01
2.	**MEMS Materials and Fabrication**: Bulk micromachining, surface micromachining, deep reactive ion etching (DRIE), wafer bonding (anodic, fusion, and direct), lithography techniques, LIGA process, thin-film deposition (CVD, PVD, sputtering), properties of MEMS materials (silicon, polymers, ceramics, metals), and scaling laws in MEMS.	08
3.	**MEMS Devices and Applications**: Micro-actuators (thermal, piezoelectric, electromagnetic), micro-sensors (chemical, pressure, optical), RF MEMS (switches, filters, resonators), accelerometers, gyroscopes, bioMEMS (lab-on-chip), microfluidic devices, energy harvesters, and emerging MEMS applications in IoT and healthcare.	08
4.	**MEMS Design and Simulation**: Multiphysics simulations (thermal, mechanical, and electrical coupling), CAD tools for MEMS (COMSOL, Coventor, ANSYS), finite element modeling (FEM), lumped parameter models, parameter extraction, MEMS packaging constraints, and design case studies (pressure sensors, accelerometers).	08
5.	**Microelectronics and MEMS Integration**: MEMS packaging techniques (wafer-level packaging, chip-scale packaging), interconnects (TSVs, wire bonding), hybrid MEMS-IC integration, reliability analysis, thermal management, failure mechanisms in MEMS, and MEMS testing methods (optical, electrical, and mechanical).	08
6.	**Emerging Areas in MEMS**: Nano-Electro-Mechanical Systems (NEMS), quantum MEMS, soft MEMS, wearable MEMS, MEMS for space applications, MEMS in robotics (haptic feedback, micro-grippers), advanced manufacturing techniques (3D printing for MEMS), and AI-enabled MEMS devices.	08

Text/Reference Books

1. **Gabriel M. Rebeiz**, *RF MEMS: Theory, Design, and Technology*, 1st Edition, Wiley-Interscience.
   - Specialized focus on RF MEMS and their design considerations.
2. **Stephen D. Senturia**, *Microsystem Design*, 1st Edition, Springer.
   - A detailed introduction to microsystem technologies and their design.
3. **Chang Liu**, *Foundations of MEMS*, 2nd Edition, Pearson.
   - Covers all essential MEMS concepts with practical examples.
4. **Marc Madou**, *Fundamentals of Microfabrication and Nanotechnology*, 3rd Edition, CRC Press.
   - Comprehensive exploration of MEMS fabrication processes and materials.
5. **Nadim Maluf and Kirt Williams**, *An Introduction to Microelectromechanical Systems Engineering*, 2nd Edition, Artech House.
   - An accessible introduction to MEMS with engineering focus.

Course Outcomes (COs)

CO	Description
CO1	Understand MEMS materials, fabrication processes, and their applications.
CO2	Analyze and design micro-scale sensors, actuators, and other MEMS devices for various domains.
CO3	Utilize simulation tools for the design, analysis, and optimization of MEMS devices.
CO4	Integrate MEMS with microelectronics for hybrid system designs and evaluate packaging and reliability challenges.
CO5	Explore advanced and emerging trends in MEMS, including NEMS and AI-integrated systems.

Course Description

This course introduces the fundamental principles, materials, and fabrication techniques of MEMS. Students will learn to analyze, design, and simulate micro-scale devices such as sensors and actuators, integrating them with electronic systems while exploring advanced trends like NEMS and AI-based systems.

Course Objectives

1. Provide a foundational understanding of MEMS materials, fabrication processes, and their applications.
2. Enable students to analyze and design micro-scale devices, including sensors and actuators.
3. Develop skills in using simulation tools for MEMS device design and optimization.

4. Explore integration techniques of MEMS with electronics, addressing packaging and reliability challenges.
5. Introduce students to emerging trends such as NEMS and AI-enhanced systems.

Mapping Table

The mapping table uses a scale of 1 to 3 to indicate the level of correlation between COs and POs/PSOs, where:

1. Slight (Low)
2. Moderate (Medium)
3. Substantial (High)

CO-PO Mapping

Course Outcomes (CO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	2	1	2	-	1	-	-	-	-	2
CO2	3	3	3	2	3	-	1	-	2	-	-	3
CO3	3	3	3	3	3	-	-	-	2	-	2	3
CO4	3	3	3	3	3	2	1	-	2	2	3	3
CO5	3	3	3	3	3	2	3	-	2	2	2	3

CO-PSO Mapping

Course Outcomes (CO)	PSO1	PSO2	PSO3
CO1	3	2	2
CO2	3	3	2
CO3	3	3	3
CO4	3	3	3
CO5	3	3	3

UNIVERSITY OF TECHNOLOGY, JAIPUR

1st Year - I Semester: M. Tech. (VLSI Design)

Lab: VLSI Physical Design Lab

Credit: 2 **Max. Marks**: 100(IA:60, ETE:40)

0L+0T+4P

S.No.	Practical Name
1.	Introduction to the various VLSI design tools (Cadence, Synopsys, Mentor Graphics) and their interface. Setting up design environment for physical design.
2.	Learn to create and set up technology files required for VLSI physical design using the specified tools.
3.	Practical on floorplanning of an integrated circuit (IC), placing macro cells, and planning the power distribution network (PDN).
4.	Learn cell placement techniques including standard cell placement and optimization in physical design flow.
5.	Design and synthesis of clock trees in VLSI circuits for optimal timing and low skew.
6.	Understanding and implementation of routing algorithms (global and detailed routing) to connect the placed cells.
7.	Performing Design Rule Checking (DRC) and Layout vs. Schematic (LVS) verification to ensure compliance with physical and electrical rules.
8.	Analysis and optimization for power and signal integrity in physical designs to minimize power consumption and ensure signal reliability.
9.	Perform static timing analysis and timing optimization to meet the timing constraints of the design.
10.	Final verification of the floorplan, placement, and routing to ensure all design constraints are met. Sign-off the design for fabrication.

UNIVERSITY OF TECHNOLOGY, JAIPUR
Scheme and Syllabus
M.Tech 1st Year, II Sem: VLSI Design

Teaching and Examination Scheme
ACADEMIC SESSION 2023-2024

S. No.	Course Name	Contact Hours per Week			Marks				Cr
		L	T	P	Exam Hrs	IA	ETE	Total	
1	Digital Signal Processing	5	0	0	3	25	100	125	5
2	Analog & Mixed Signal ICs	5	0	0	3	25	100	125	5
3	CAD of ICs	5	0	0	3	25	100	125	5
4	Biomedical Electronics	5	0	0	3	25	100	125	5
5	Digital System Design Lab	0	0	4		60	40	100	2
	Total	**20**	**0**	**4**		**160**	**440**	**600**	**22**

***L:** Lecture, **T:** Tutorial, **P:** Practical, **Cr:** Credits*
***ETE:** End Term Exam, **IA:** Internal Assessment*
***: Not to be considered for award of division*

1st Year - II Semester: M. Tech. (VLSI Design)

Sub: Digital Signal Processing

Credit: 5 **Max. Marks**: 125 (IA:25, ETE:100)

5L+0T+0P **End Term Exam**: 3 Hours

S.No.	CONTENTS	CONTACT HOURS
1.	**Introduction**: Objective, scope, and outcome of the course.	1
2.	**Discrete-Time Signals and Systems**: Overview of DSP systems, basic concepts in signal processing. Signal processing in communications, audio, and image applications. Classification of signals, discrete-time systems, linear shift-invariant systems, convolution, difference equations, sampling, quantization, and reconstruction of signals. Discrete-time system properties, impulse response, step response.	7
3.	**Z-Transforms**: Definition, properties, inverse Z-transform, region of convergence, applications in solving difference equations, system stability, rational Z-transform, region of stability, and partial fraction expansion.	7
4.	**Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT)**: DFT, properties, relationship to the Fourier series, FFT algorithms (Cooley-Tukey), Radix-2, applications of DFT in spectral analysis, Goertzel algorithm, decimation in time and frequency.	8
5.	**Digital Filter Design**: FIR filters, IIR filters, filter structures (direct, cascade, and parallel), Butterworth, Chebyshev, and elliptic filters, filter design using windowing and frequency sampling, Parks-McClellan algorithm, multirate filtering.	8
6.	**Applications of DSP**: Audio and speech processing, image processing, communications, filter banks, noise reduction, speech enhancement, real-time DSP systems, ECG signal processing, speech synthesis.	8

Text/Reference Books:

1. **John G. Proakis**, "Digital Signal Processing: Principles, Algorithms, and Applications," 4th Edition.
2. **Alan V. Oppenheim**, "Discrete-Time Signal Processing," 3rd Edition.
3. **Sanjay Sharma**, "Digital Signal Processing: Theory and Applications," PHI.
4. **Ramesh Babu**, "Digital Signal Processing," Pearson.

Course Outcomes (COs)

CO No.	Course Outcomes (COs)
CO1	Understand the fundamental concepts of discrete-time signals, systems, and sampling.
CO2	Apply Z-Transforms for analyzing and solving discrete-time system problems.
CO3	Implement DFT and FFT algorithms for spectral analysis of signals.
CO4	Design and implement FIR and IIR filters for digital signal processing applications.
CO5	Use DSP techniques in real-world applications like speech, image processing, and communications.

Course Description

Digital Signal Processing (DSP) focuses on the mathematical and algorithmic tools used to analyze, design, and implement signal processing systems. It covers discrete-time signals, sampling, Z-transforms, DFT, FFT, and filter design, emphasizing real-world applications like speech, image processing, and communication systems.

Course Objectives

1. To understand the fundamental principles and techniques of Digital Signal Processing.
2. To analyze and design discrete-time systems using Z-transforms and Fourier analysis.
3. To implement and evaluate digital filters (FIR and IIR) for various applications.
4. To apply DSP algorithms to real-world scenarios, enhancing problem-solving and critical thinking skills.

Mapping Table

The mapping table uses a scale of 1 to 3 to indicate the level of correlation between COs and POs/PSOs, where:

1. Slight (Low)
2. Moderate (Medium)
3. Substantial (High)

CO-PO Mapping

Course Outcomes (CO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	2	2	-	-	-	-	-	-	2
CO2	3	3	2	2	2	-	-	-	-	-	-	2
CO3	3	3	3	3	3	-	-	-	-	2	-	2
CO4	3	3	3	3	3	2	2	-	-	-	2	2
CO5	3	3	3	3	3	3	3	-	-	3	2	3

CO-PSO Mapping

Course Outcomes (CO)	PSO1	PSO2	PSO3
CO1	3	2	1
CO2	3	3	2
CO3	3	3	3
CO4	3	3	3
CO5	3	3	3

UNIVERSITY OF TECHNOLOGY, JAIPUR

1st Year - II Semester: M. Tech. (VLSI Design)

Sub: Analog & Mixed Signal ICs

Credit: 5 **Max. Marks**: 125 (IA:25, ETE:100)

5L+0T+0P **End Term Exam**: 3 Hours

S.No.	CONTENTS	CONTACT HOURS
1.	**Introduction**: Objective, scope, and outcome of the course.	1
2.	**Analog IC Design**: Basics of analog and mixed-signal IC design, challenges, and applications, Operational amplifiers (Op-Amps), differential amplifiers, frequency response, feedback in analog circuits, stability analysis, frequency compensation techniques, noise analysis, slew rate, offset voltage, and drift.	7
3.	**Mixed-Signal Circuit Design**: Analog-to-digital converters (ADC), digital-to-analog converters (DAC), oversampling, noise shaping, pipelined ADC, sigma-delta ADC, applications in data conversion, and interleaved ADCs.	8
4.	**Feedback and Stability in Analog Circuits**: Types of feedback, stability criteria, loop gain, pole-zero placement, Nyquist and Bode criteria, compensation techniques, open-loop and closed-loop systems, frequency-domain stability analysis.	7
5.	**CMOS Analog Circuit Design**: CMOS transistor-level design, CMOS current mirrors, differential pairs, active loads, current sources, voltage regulators, operational amplifier design using CMOS, low-voltage analog circuits.	8
6.	**Low Power Design and Advanced Topics**: Low-power design techniques, scaling laws in CMOS, low-voltage analog circuits, design for noise immunity, mixed-signal integration, RF circuits in CMOS, noise reduction techniques in mixed-signal ICs.	8

Text/Reference Books:

1. **Behzad Razavi**, "Design of Analog CMOS Integrated Circuits," 2nd Edition.
2. **David A. Johns**, Ken Martin, "Analog Integrated Circuit Design," 2nd Edition.
3. **Paul R. Gray**, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits," 5th Edition.
4. **Jacob Baker**, "CMOS: Circuit Design, Layout, and Simulation," 3rd Edition.

Course Outcomes (COs)

CO No.	Course Outcomes (COs)
CO1	Understand the design principles of analog ICs, particularly op-amps and differential amplifiers.
CO2	Design and analyze ADCs, DACs, and other mixed-signal circuits.
CO3	Understand feedback mechanisms in analog circuits and design stable systems.
CO4	Design CMOS analog circuits and analyze their performance.
CO5	Apply low-power design techniques and advanced topics in analog and mixed-signal ICs.

Course Description

This course on Analog & Mixed Signal ICs introduces the principles of analog circuit design, focusing on operational amplifiers, feedback systems, and mixed-signal components like ADCs and DACs. It emphasizes CMOS design, low-power techniques, and applications in modern electronic systems.

Course Objectives

1. To understand the working principles of analog ICs and their building blocks.
2. To analyze and design mixed-signal circuits such as ADCs and DACs.
3. To explore feedback mechanisms and their role in designing stable analog circuits.
4. To apply low-power and advanced design techniques in CMOS analog and mixed-signal ICs.

Mapping Table

The mapping table uses a scale of 1 to 3 to indicate the level of correlation between COs and POs/PSOs, where:

1. Slight (Low)
2. Moderate (Medium)
3. Substantial (High)

CO-PO Mapping

Course Outcomes (CO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	2	2	-	-	-	-	-	-	2
CO2	3	3	3	3	3	-	-	-	-	-	-	2
CO3	3	3	2	2	2	-	2	-	-	2	-	2
CO4	3	3	3	3	3	2	2	-	-	-	2	2
CO5	3	3	3	3	3	3	3	-	-	3	2	3

CO-PSO Mapping

Course Outcomes (CO)	PSO1	PSO2	PSO3
CO1	3	2	1
CO2	3	3	3
CO3	3	3	2
CO4	3	3	3
CO5	3	3	3

UNIVERSITY OF TECHNOLOGY, JAIPUR

1st Year - II Semester: M. Tech. (VLSI Design)

Sub: CAD of ICs

Credit: 5 **Max. Marks**: 125 (IA:25, ETE:100)

5L+0T+0P **End Term Exam**: 3 Hours

S.No.	CONTENTS	CONTACT HOURS
1.	**Introduction**: Objective, scope, and outcome of the course.	1
2.	**Fundamentals of IC Design**: Introduction to the CAD tools and the IC design flow. Design methodologies, design for manufacturability, design for testability, Basic concepts in digital and analog IC design, design tools overview, process technology, design rules, layout concepts, fabrication processes, standard cell libraries, and design automation.	7
3.	**Physical Design Automation**: Floorplanning, placement, routing, signal integrity, wirelength minimization, clock distribution, power grid design, routing algorithms, chip power and thermal management.	8
4.	**Design Verification and Testing**: Timing analysis, design rule checking (DRC), layout versus schematic (LVS), parasitic extraction, fault simulation, and test pattern generation, ATPG, fault coverage.	8
5.	**Power Analysis and Optimization**: Power dissipation in CMOS circuits, techniques for low-power design, dynamic and static power, voltage scaling, power optimization at the circuit and system levels, clock gating, power management units.	8
6.	**Advanced Topics**: VLSI CAD tools for system-on-chip (SoC) design, yield analysis, design for manufacturability (DFM), design for testability (DFT), emerging technologies in IC design, quantum computing design, 3D IC integration.	8

Text/Reference Books:

1. **Carlo H. Sequin**, "VLSI Design: A Practical Introduction," 2nd Edition.
2. **Naveed Shervani**, "Design Automation for Analog and Mixed-Signal Circuits."

3. **Neil H. E. Weste**, “Principles of CMOS VLSI Design: A Systems Perspective (VLSI Systems Series)” Hardcover – 1 May 1993
4. **M. J. S. Smith**, "Digital Integrated Circuits: A Design Perspective," 2nd Edition.

Course Outcomes (COs):

CO No.	Course Outcomes (COs)
CO1	Understand the fundamentals of IC design and the role of CAD tools in the design process.
CO2	Apply physical design automation techniques in placement, routing, and layout.
CO3	Perform design verification and testing through tools like DRC, LVS, and timing analysis.
CO4	Optimize power consumption in IC design through various power analysis techniques.
CO5	Implement advanced CAD tools and methods for SoC design, manufacturability, and yield improvement.

Course Description

This course focuses on the **CAD of ICs**, covering the principles and techniques of physical design automation, verification, and testing in VLSI systems. It emphasizes the use of modern CAD tools for optimization, layout design, and ensuring manufacturability and yield.

Course Objectives

1. To understand the role and significance of CAD tools in IC design.
2. To learn and apply physical design techniques, including placement, routing, and layout generation.
3. To explore verification techniques such as DRC, LVS, and timing analysis.
4. To optimize power and performance in IC designs while considering manufacturability.

Mapping Table

The mapping table uses a scale of 1 to 3 to indicate the level of correlation between COs and POs/PSOs, where:

1. Slight (Low)
2. Moderate (Medium)
3. Substantial (High)

CO-PO Mapping

Course Outcomes (CO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	2	3	-	-	-	-	-	-	2
CO2	3	3	3	3	3	-	-	-	-	-	2	2
CO3	3	3	3	3	3	-	-	-	-	2	2	2
CO4	3	3	3	3	3	2	3	-	-	-	2	3
CO5	3	3	3	3	3	3	3	-	-	2	2	3

CO-PSO Mapping

Course Outcomes (CO)	PSO1	PSO2	PSO3
CO1	3	-	-
CO2	2	2	1
CO3	1	-	-
CO4	2	1	3
CO5	3	2	3

UNIVERSITY OF TECHNOLOGY, JAIPUR

1st Year - II Semester: M. Tech. (VLSI Design)

Sub: Biomedical Electronics

Credit: 5 **Max. Marks**: 125 (IA:25, ETE:100)

5L+0T+0P **End Term Exam**: 3 Hours

S.No.	CONTENTS	CONTACT HOURS
1.	**Introduction**: Objective, scope, and outcome of the course. Overview of biomedical signals and instruments, the importance of biomedical instrumentation in healthcare.	1
2.	**Biomedical Instrumentation**: Measurement of bio-signals (ECG, EEG, EMG), biopotential electrodes, amplifiers, and signal conditioning. Electrocardiograph (ECG) system, electroencephalograph (EEG), electromyograph (EMG).	8
3.	**Medical Imaging Systems**: X-ray, CT scan, MRI, ultrasound, optical imaging techniques. Image processing for medical applications, medical image compression, and reconstruction algorithms.	8
4.	**Patient Monitoring Systems**: ECG monitoring, pulse oximetry, blood pressure monitoring, respirators, and ventilators, home-based monitoring devices, IoT in healthcare.	8
5.	**Bioelectric Signal Processing**: Noise in bioelectrical signals, filtering techniques, detection of anomalies in bio-signals, real-time signal processing for medical devices.	8
6.	**Advanced Applications and Trends**: Telemedicine, wearable devices, biomedical sensors, artificial organs, medical robotics, biotechnology in electronics, neural prosthetics, and brain-computer interfaces.	8

Text/Reference Books:

1. **J. J. Carr**, "Introduction to Biomedical Equipment Technology," 5th Edition.
2. **R. S. Khandpur**, "Handbook of Biomedical Instrumentation," 3rd Edition.

3. **Leslie Cromwell**, "Biomedical Instrumentation and Measurement," 2nd Edition.
4. **Michael H. Tooley**, "Biomedical Engineering: Principles and Applications."

Course Outcomes (COs):

CO No.	Course Outcomes (COs)
CO1	Understand the working of basic biomedical instrumentation systems.
CO2	Analyze and process bioelectric signals such as ECG, EEG, and EMG.
CO3	Apply medical imaging techniques and technologies for diagnostics.
CO4	Design and develop patient monitoring systems for healthcare.
CO5	Explore emerging trends in biomedical electronics, including wearable and implantable devices.

Course Description

This course introduces the fundamentals of **biomedical electronics**, focusing on the design, analysis, and application of instrumentation systems in healthcare. Students will explore bioelectric signals, medical imaging, patient monitoring systems, and emerging trends such as wearable and implantable devices.

Course Objectives

1. To understand the principles and working of biomedical instrumentation systems.
2. To analyze bioelectric signals like ECG, EEG, and EMG for diagnostics.
3. To explore medical imaging techniques and their applications in healthcare.
4. To design and develop innovative patient monitoring systems.
5. To examine emerging technologies in biomedical electronics, such as wearable devices.

Mapping Table

The mapping table uses a scale of 1 to 3 to indicate the level of correlation between COs and POs/PSOs, where:

1. Slight (Low)
2. Moderate (Medium)
3. Substantial (High)

CO-PO Mapping

Course Outcomes (CO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	2	3	-	-	-	-	-	-	2
CO2	3	3	3	3	3	2	-	-	-	-	-	2
CO3	3	3	3	3	3	2	3	-	-	-	-	2
CO4	3	3	3	3	3	3	3	2	-	2	2	3
CO5	3	3	3	3	3	3	3	2	-	2	2	3

CO-PSO Mapping

Course Outcomes (CO)	PSO1	PSO2	PSO3
CO1	3	2	1
CO2	3	3	2
CO3	3	3	3
CO4	3	3	3
CO5	3	3	3

1st Year - II Semester: M. Tech. (VLSI Design)

Lab: Digital System Design Lab

Credit: 2 **Max. Marks**: 100(IA:60, ETE:40)

0L+0T+4P

S.No.	Practical Title
1.	Learn the basics of VHDL/Verilog syntax, writing simple modules, and simulation of basic logic gates.
2.	Design and implement combinational circuits such as adders, subtractors, multipliers, and dividers using VHDL/Verilog.
3.	Design and implement sequential circuits such as flip-flops (SR, JK, D, T), counters (up/down counters), and shift registers.
4.	Design and simulate 2-to-1, 4-to-1, and 8-to-1 multiplexers, as well as demultiplexers, using VHDL/Verilog.
5.	Implement binary to BCD, gray code to binary, and other code converters using VHDL/Verilog.
6.	Design and simulate FSMs (Mealy and Moore) for applications like sequence detector, traffic light controller, etc., using VHDL/Verilog.
7.	Design an Arithmetic Logic Unit (ALU) capable of performing arithmetic and logical operations (addition, subtraction, AND, OR, etc.).
8.	Design and simulate memory elements such as RAM, ROM, and FIFO buffers in VHDL/Verilog.
9.	Implement clock dividers, delay elements, and other timing circuits for real-time applications.

UNIVERSITY OF TECHNOLOGY, JAIPUR
Scheme and Syllabus
M.Tech 2nd Year, III Sem: VLSI Design

Teaching and Examination Scheme
ACADEMIC SESSION 2023-2024

S. No.	Course Name	Contact Hours per Week			Marks				Cr
		L	T	P	Exam Hrs	IA	ETE	Total	
1	Embedded System Design	5	0	0	3	25	100	125	5
2	VLSI Testing & Testability	5	0	0	3	25	100	125	5
3	Seminar	0	0	0		90	60	150	6
4	Dissertation- I	0	0	0		100	0	100	4
	Total					**240**	**260**	**500**	**20**

L: *Lecture,* ***T:*** *Tutorial,* ***P:*** *Practical,* ***Cr:*** *Credits*
ETE: *End Term Exam,* ***IA:*** *Internal Assessment*
**: Not to be considered for award of division*

UNIVERSITY OF TECHNOLOGY, JAIPUR

2nd Year - III Semester: M. Tech. (VLSI Design)

Sub: Embedded System Design

Credit: 5 **Max. Marks**: 125 (IA:25, ETE:100)

5L+0T+0P **End Term Exam**: 3 Hours

S.No.	**CONTENTS**	**CONTACT HOURS**
1.	**Introduction**: Objective, scope, and outcome of the course.	1
2.	**Embedded System Architecture**: Overview of embedded systems, applications in real-time systems, and hardware/software co-design. Introduction to microcontrollers and embedded programming. Architecture of embedded systems, microprocessor and microcontroller architectures, embedded processors, system-on-chip (SoC), and multi-core processors. Memory hierarchy: RAM, ROM, EEPROM, Flash, memory-mapped I/O.	5
3.	**Programming Embedded Systems**: Programming techniques in C, assembly language programming, handling interrupts, real-time operating systems (RTOS), task scheduling, inter-process communication, synchronization, and semaphores.	7
4.	**Input/Output Interfacing and Devices**: Interfacing with external devices, ADC/DAC, digital I/O, UART, SPI, I2C, GPIO, timers, and real-time clock (RTC). Sensor interfacing (temperature, humidity, accelerometer), actuators (motors, LEDs), and power management.	6
5.	**Embedded System Design Tools**: Development tools for embedded systems, compilers, debuggers, simulators, hardware description languages (HDL), debugging techniques, and performance analysis tools. Introduction to FPGA-based embedded systems.	7
6.	**Embedded System Applications and Case Studies**: Embedded system design for communication, medical devices, automotive systems, industrial automation, robotics, IoT devices, and smart homes. Case studies of embedded systems in action.	6

Text/Reference Books:

1. **Raj Kamal**, "Embedded Systems: Architecture, Programming and Design," 3rd Edition.
2. **Wayne Wolf**, "Computers as Components: Principles of Embedded Computing System Design," 2nd Edition.
3. **David E. Simon**, "An Embedded Software Primer," 1st Edition.
4. **Steven Barrett**, "Embedded Systems: A Contemporary Design Tool," Pearson.

Course Outcomes (COs)

CO No.	Course Outcomes (COs)
CO1	Understand the architecture of embedded systems and various components involved in embedded design.
CO2	Design and program embedded systems using C and assembly language with real-time constraints.
CO3	Interface embedded systems with various I/O devices, sensors, and actuators for real-world applications.
CO4	Use embedded system design tools to develop and debug embedded systems, including hardware and software integration.
CO5	Apply embedded system design techniques to solve practical problems in applications such as IoT, automotive, and medical systems.

Course Description

The Embedded System Design course covers the fundamentals of embedded systems, including their architecture and key components. Students will learn to design and program embedded systems using C and assembly languages while interfacing with various I/O devices, sensors, and actuators, for real-world applications like IoT, automotive, and medical systems.

Course Objectives

1. To understand the architecture and components involved in embedded system design.
2. To design and program embedded systems using C and assembly language while considering real-time constraints.
3. To interface embedded systems with I/O devices, sensors, and actuators for practical applications.
4. To use embedded system design tools for development, debugging, and hardware/software integration.
5. To apply embedded system design techniques in real-world applications, including IoT, automotive, and medical systems.

Mapping Table

The mapping table uses a scale of 1 to 3 to indicate the level of correlation between COs and POs/PSOs, where:

1. Slight (Low)
2. Moderate (Medium)
3. Substantial (High)

CO-PO Mapping

Course Outcomes (CO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	2	3	1	1	-	-	2	2	2
CO2	3	3	3	3	3	2	1	-	-	3	2	3
CO3	3	3	3	3	3	2	2	-	-	3	3	3
CO4	3	3	3	3	3	3	3	2	-	3	2	3
CO5	3	3	3	3	3	3	3	2	1	3	3	3

CO-PSO Mapping

Course Outcomes (CO)	PSO1	PSO2	PSO3
CO1	3	2	1
CO2	3	3	2
CO3	3	3	3
CO4	3	3	3
CO5	3	3	3

UNIVERSITY OF TECHNOLOGY, JAIPUR

2nd Year - III Semester: M. Tech. (VLSI Design)

Sub: VLSI Testing & Testability

Credit: 5 **Max. Marks**: 125 (IA:25, ETE:100)

5L+0T+0P **End Term Exam**: 3 Hours

S.No.	CONTENTS	CONTACT HOURS
1.	**Introduction**: Objective, scope, and outcome of the course.	1
2.	**Test Generation for Digital Circuits**: Overview of VLSI design, testing challenges, testability concepts, and the role of testing in the VLSI design process. Fault models (stuck-at faults, bridging faults, delay faults), test pattern generation, deterministic and random testing, D-algorithm, PODEM, and ATPG. Functional and structural testing.	8
3.	**Testability Measures**: Observability and controllability, testability analysis, scan-based testing, design-for-testability (DFT) techniques, scan chains, boundary scan, and built-in self-test (BIST).	8
4.	**Built-In Self-Test (BIST)**: Concepts, BIST architectures, BIST for digital circuits, test generation algorithms for BIST, compression techniques in BIST, DFT techniques for analog and mixed-signal circuits.	8
5.	**Fault Simulation and Diagnosis**: Fault simulation techniques, fault simulation tools, fault coverage analysis, diagnosis of defective circuits, fault localization techniques. Statistical methods in fault diagnosis.	7
6.	**Advanced Topics in VLSI Testing**: Delay testing, power testing, testing for deep sub-micron designs, testing at high frequencies, memory testing, analog and mixed-signal testing, fault tolerance in VLSI systems, emerging trends in VLSI testing.	8

Text/Reference Books:

1. **M. Bushnell**, **V. D. Agrawal**, "Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits," Springer.

2. **Aditya P. Mehta**, "VLSI Design and Test," Pearson.
3. **Wayne Wolf**, "Modern VLSI Design: Systems on Chip," 4th Edition.
4. **R. K. Gupta**, "VLSI Design and Test," Oxford University Press.

Course Outcomes (COs)

CO No.	Course Outcomes (COs)
CO1	Understand the principles of VLSI testing and the various fault models in digital circuits.
CO2	Develop test patterns for VLSI circuits using test generation algorithms.
CO3	Apply DFT techniques to improve the testability of VLSI circuits.
CO4	Implement BIST and fault simulation techniques to evaluate and diagnose VLSI designs.
CO5	Address advanced testing issues in VLSI, such as delay testing, power testing, and analog/mixed-signal testing.

Course Description

The VLSI Testing & Testability course focuses on the principles and techniques used to test Very Large-Scale Integration (VLSI) circuits. Students will learn fault models, test generation algorithms, and design-for-test (DFT) methods. The course covers Built-In Self-Test (BIST), fault simulation, and advanced testing issues such as delay, power, and mixed-signal testing, which are crucial for ensuring the reliability of VLSI designs.

Course Objectives

1. To understand the principles of VLSI testing and various fault models in digital circuits.
2. To develop test patterns for VLSI circuits using test generation algorithms.
3. To apply Design for Testability (DFT) techniques to enhance the testability of VLSI circuits.
4. To implement Built-In Self-Test (BIST) and fault simulation techniques for evaluating and diagnosing VLSI designs.
5. To address advanced VLSI testing challenges such as delay testing, power testing, and analog/mixed-signal testing.

Mapping Table

The mapping table uses a scale of 1 to 3 to indicate the level of correlation between COs and POs/PSOs, where:

1. Slight (Low)
2. Moderate (Medium)
3. Substantial (High)

CO-PO Mapping

Course Outcomes (CO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	3	2	-	-	-	-	-	1	-	1
CO2	3	1	3	3	1	-	1	-	-	-	-	-
CO3	2	3	-	2	-	-	2	-	-	-	-	2
CO4	2	1	3	2	2	-	-	-	-	-	-	1
CO5	3	2	-	2	3	-	-	-	-	-	-	3

CO-PSO Mapping

Course Outcomes (CO)	PSO1	PSO2	PSO3
CO1	3	-	-
CO2	2	2	2
CO3	-	1	-
CO4	1	2	3
CO5	3	2	3